Simulation of Ultrafast All-Optical XOR Gate with SOA-Based UNI and Cascaded ODI

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***Abstract*—The feasibility of employing an optical delay interferometer (ODI) to double the data rate of the conventional semiconductor optical amplifier-based ultrafast nonlinear interferometer configured as XOR gate is theoretically investigated and demonstrated. The numerical simulation conducted for this purpose allows to find the optimum temporal offset that must be inserted by the cascaded ODI in order to realize the specific Boolean function both with error-free and pattern-free performance.**

I. INTRODUCTION

The execution of all-optical XOR logic is crucial toward signal processing exclusively in the optical domain [1]. One option for doing this is by employing the semiconductor optical amplifier (SOA)-based ultrafast nonlinear interferometer (UNI) [2]. However, as the bandwidth demand in modern photonic networks is rapidly increasing due to the massive use of broadband applications, it is necessary that its working rate scales accordingly to satisfy this need. In this effort several modified versions of its standard architecture have been proposed [3-4], but faster XOR operation has been achieved at the cost of increased complexity and rather tricky adjustment of the corresponding setups. A more affordable and practical way to deal with this issue at the current running data rates is to serially connect to the gate's output an optical delay interferometer (ODI) [5]. Therefore in this paper we investigate the feasibility of this idea for the conventional SOA-based UNI configured as XOR gate, where due to the single arm geometry the strain imposed on the SOA gain dynamics is inherently heavier as opposed to other similar schemes [5]. For this purpose we formulate in Section II a model to describe and link the operation of the concatenated modules. The conducted simulation enables to investigate the impact of the time delay inserted by the ODI and find the value that is most suitable to realize the XOR function at doubled rate compared to [2] both with bitwise logical correctness and high quality, according to the details in Section III.

II. MODELLING

Fig. 1 depicts the block diagram of the simulated setup. The amount of the clock signal (CLK) with power $P_{CLK}(t)$ that is switched at port O1 of the SOA-based UNI from the XOR operation between the binary content of control signals A and B is given by (1) [2], where $\alpha = 8$ is the SOA alpha factor while $G_R(t) = G_f(t)/G_s(t-T_{delay})$ is the ratio of the gains suffered by the clock copies, which are temporally separated by T_{delay} = 12.5 ps:

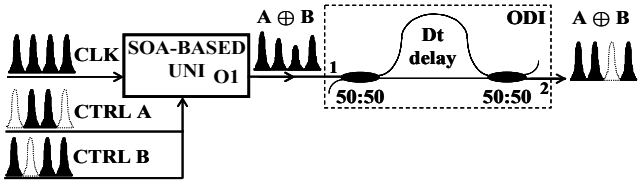

Figure 1. Simulated setup

$$P_{O1}(t) = \frac{1}{4} G_s(t-T_{delay}) \left\{ 1 + G_R(t) - 2\sqrt{G_R(t)} \cos\left[-\frac{\alpha}{2} \ln G_R(t) \right] \right\} P_{CLK}(t) \quad (1)$$

and its phase by the analytical expression [6]

$$\varphi_{O1}(t) = -\frac{\alpha}{2} G_s(t-T_{delay}) + \arctan\left[\frac{\sqrt{G_R(t)} \sin\left(\frac{\alpha}{2} \ln G_R(t) \right)}{1 - \sqrt{G_R(t)} \cos\left(\frac{\alpha}{2} \ln G_R(t) \right)} \right] \quad (2)$$

The involved gains are determined, via $G_f(t) = \exp\left[h_A(t) \right]$ and $G_s(t) = \exp\left[h_B(t) \right]$, by the SOA response, $h_i(t)$, to the injected data pulses of power $P_{CTRL,\,i}(t)$ [2]

$$\frac{dh_i(t)}{dt} = \frac{1}{1 + \varepsilon \exp\left[h_i(t) \right] P_{CTRL,\,i}(t)} \times \left\{ \frac{\ln(G_{ss}) - h_i(t)}{T_{carrier}} - \varepsilon \left[\exp\left(h_i(t) \right) - 1 \right] \frac{dP_{CTRL,\,i}(t)}{dt} - \left[\exp\left(h_i(t) \right) - 1 \right] P_{CTRL,\,i}(t) \left(\frac{\varepsilon}{T_{carrier}} + \frac{1}{E_{sat}} \right) \right\} \quad (3)$$

where the subscript "*i*" denotes either control A or B and G_{ss}, $T_{carrier}$, ε = 0.2 W^{-1} and E_{sat} = 1 pJ are the SOA small signal gain, carrier lifetime, nonlinear gain compression factor and saturation energy, respectively. Now when a signal is launched from port 1 into an ODI whose arms have a relative delay Dt then the resultant power at port 2 is [7]

$$P_{ODI}(t) = \frac{1}{4} \left\{ P_{O1}(t) + P_{O1}(t-Dt) + 2\sqrt{P_{O1}(t) P_{O1}(t-Dt)} \times \cos\left[\varphi_{O1}(t) - \varphi_{O1}(t-Dt) \right] \right\} \quad (4)$$

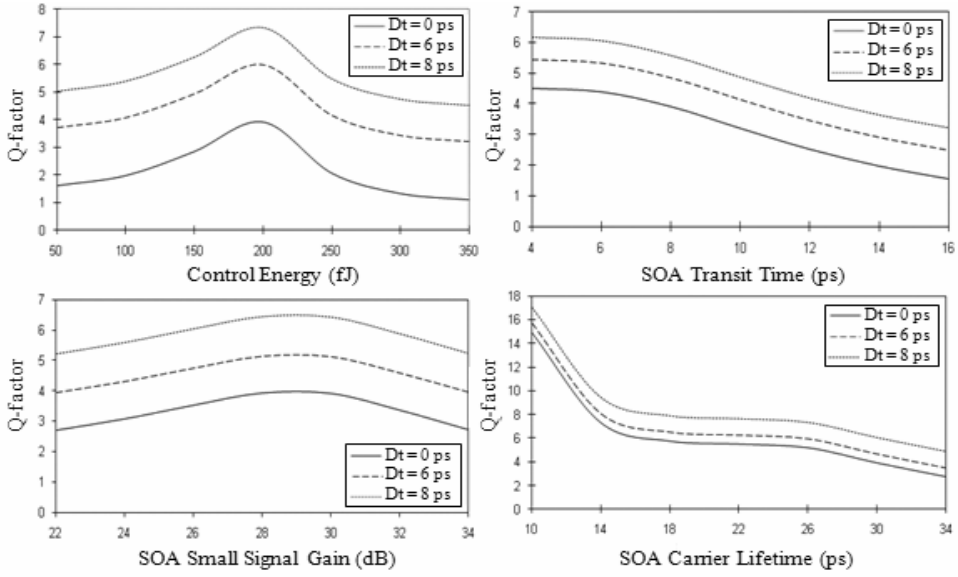

Figure 2. Q-factor variation vs. critical parameters

III. RESULTS

The performance of the scheme is evaluated at 40 Gb/s by means of the variation of the Q-factor [2], which for error-free operation must be at least over six, against the most critical parameters. The results, which have been obtained after (3) was numerically solved according to the details in [2] for Gaussian-shaped input signals of full-width at half-maximum 7 ps, are depicted in Fig. 2. Their observation reveals that without the ODI, i.e. Dt = 0 ps, it is not possible to meet the minimum requirement for the Q-factor for all the critical parameters but the SOA carrier lifetime. However the demand for the latter is very tight, as it should be smaller than the considered pulse repetition interval by 37%, at the expense of employing gain recovery acceleration techniques with their associated technical difficulties mentioned in [2]. The ODI instead relaxes this requirement while the adjustment of its time delay to about $1/3^{rd}$ of the operating period opens concurrently a range of parameters values for which Q > 6. In fact, by combining Dt = 8 ps with 200 fJ, 6 ps, 28 dB and 25 ps for the data energy and SOA transit time, small signal gain and carrier lifetime, respectively, then as it can be seen in Fig. 3 the XOR function can be executed between the representative data frames of 01101001 (a) and 10110011 (b) both with bitwise logical correctness and high quality (c). In contrast if the ODI is not used then this is not possible with the same set of values, since logical errors occur, as it happens in the 3^{rd} and 8^{th} bit slots, while the '1's are much less uniform (d).

IV. CONCLUSION

The capability of an ODI to double from the previous one the operating speed of the SOA-based UNI full-pattern-operated XOR gate has been theoretically demonstrated and its time delay that is most suitable for achieving this has been specified. The proposed scheme can constitute a practical solution for extending the data rate of this switch and enabling its use as core logical unit in more complex circuits.

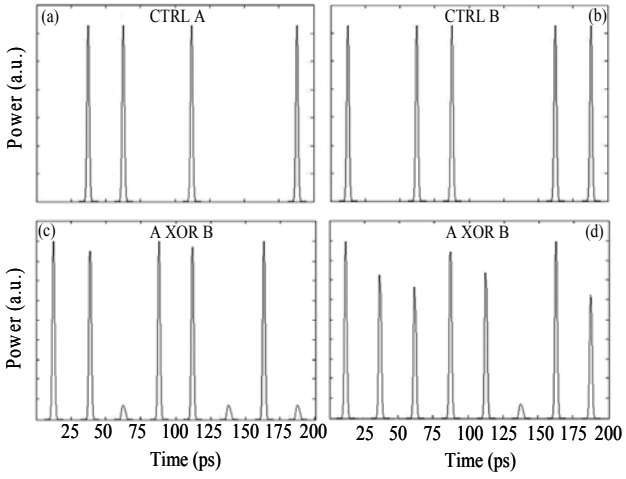

Figure 3. Simulation results

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