Circuit Model for Analysis of SOA Based Photonic Switch

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***Abstract*— An equivalent lumped element electric SPICE circuit model for traveling wave semiconductor optical amplifier has been presented using the rate equation for carriers. The model has been used to represent an all optical 2x2 switch based on cross gain modulation in SOA capable of operating at an ultra fast speed. SPICE simulation of the switch with the proposed circuit model provides bit error rate (BER) values at the output of the switch which are seen to be in close agreement with the experimentally measured values at 10Gbps. The degradation of BER performance has been examined in the presence of chip parasitic elements of SOA.**

I. INTRODUCTION

Continuously increasing data rate in optical network demands implementation of all optical packet routers. Overcoming the bottleneck of Opto Electro Optic (OEO) conversion, all optical packet switching can offer transparency to data rate and format. Semiconductor Optical Amplifiers (SOA) and nonlinear fiber based devices are most promising elements to implement all optical ultra-fast photonic switch. The latter one although provides ultra-fast switching speed but not capable of being integrated into optical network, whereas SOA can easily be integrated, cascaded and operated at low cost and power.

A number of theoretical models: both analytical and numerical have been proposed in the literature[1] for predicting operating characteristics of Traveling Wave Semiconductor Optical Amplifier (TWSOA). In this work we have presented a simple electrical equivalent circuit model of Traveling Wave SOA which we proposed in our earlier work[3]. The model has been used to represent an all optical 2x2 photonic switch. Switching performance has been investigated by calculating bit error rate (BER) at the output of the switch with received optical power. Representing an SOA with our electrical equivalent circuit model offers an opportunity to predict the effect of parasitic elements on the switching performance. Such an important study has been carried out and the effect of chip parasitics on the BER performance of the switch has been examined in the present work.

II. THEORY AND MODELING

The rate equation for carrier density in SOA can be modeled as [3]

$$\frac{eV_0}{aL\Gamma}\frac{dg_L(t)}{dt} = I(t) - \frac{eV_0}{\tau_N}N_0 - g_L(t)\left[\frac{eV_0}{aL\Gamma\tau_N}\right] - \left[\frac{e}{h\nu}P_{in}\right]e^{(g_L(t)-1)} \quad (1)$$

Where $g_L(t) = g_{dc} + \Delta g(t)$ represents sum of the dc gain and small signal ac gain, $I(t)$, V_0 and L are respectively the bias current, volume and length of the active region of SOA. Γ, a, N_0 and τ_N signify confinement factor, differential gain constant, carrier density at transparency and carrier recombination lifetime of the SOA respectively.

The equation (1) is modified to represent the following equation[3]

$$\left(\frac{eV_0}{\Gamma aL}\right)\frac{d(\Delta g)}{dt} = I - \frac{eV_0N_0}{\tau_N} - \left(\frac{eV_0}{aL\Gamma\tau_N}\right)(g_{dc}+\Delta g) - \left(\frac{eP_{tot}}{h\nu}\right)\left[e^{g_{dc}} + (e^{g_{dc}}\Delta g) - 1\right] \quad (2)$$

Ac part of equation (2) can be compared with the following circuit equation

$$C\frac{dV}{dt} = I - I_1 - I_2 - I_3(t) - \frac{V}{R} \quad (3)$$

Equation (3) can be represented by the following circuit in Fig.1.

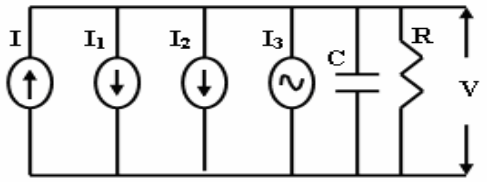

Fig.1: Electrical equivalent circuit model for ac analysis of SOA.

Description of the switch:

A 2x2 CROSS BAR switch using two identical SOAs is shown in Fig.2. IN1 and IN2 indicate input packets having same power level but different wavelengths. P1 is the pump signal consisting of a high intensity pulse train and P2 is the inverted pump. BPF1 and BPF2 are band pass filters employed to pass the frequencies of IN1 and IN2 respectively. Cross Gain Modulation (XGM) property of SOA has been utilized to implement the switching action as follows. When

P1 is at high state and P2 is at low state, SOA1 provides low gain hence its output is low because of gain saturation in SOA1. At the same time SOA2 gain is high and hence allows both IN1 and IN2 to pass through it. So input packet IN2 reaches OUT1 and IN1 reaches OUT2 thereby implying CROSS state of the switch.

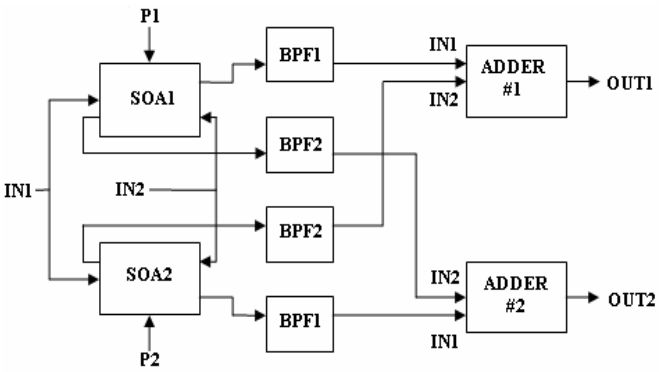

Fig.2: Representation of a 2x2 CROSS-BAR switch using equivalent circuit model.

When P1 and P2 are interchanged, SOA2 gain is low and hence it has low output. Now SOA1 gain is high and allows input packets IN1 and IN2 to pass through it. IN1 goes to OUT1 and IN2 goes to OUT2 and consequently we get BAR state of switching. In order to avoid collision between two identical wavelength packets IN1 and IN2, counter propagating inputs are applied to the SOAs and separate outputs from both ends of each SOA are connected to the input of each band pass filter.

III. RESULTS AND DISCUSSION

Using Gaussian statistics of noise, extinction ratios and BER values are calculated at the switch output at different received optical powers. Mean power level of -7dBm for the input packets and high level of pump signal at 11.5dBm have been used in the simulation. Low level of the pump is kept at 0 dBm for complete gain recovery in the SOAs.

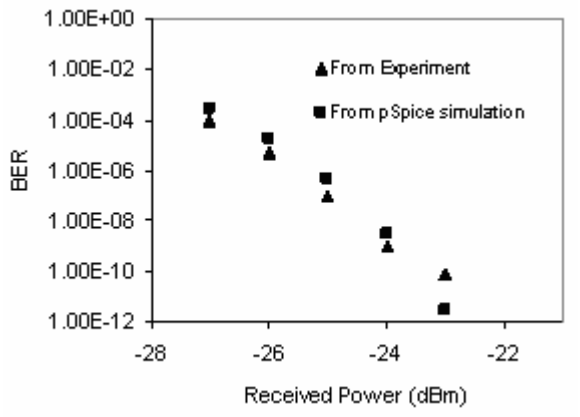

Fig.3: BER curve in CROSS and BAR state of the 2x2 all-optical switch using XGM in SOA at 10Gbps.

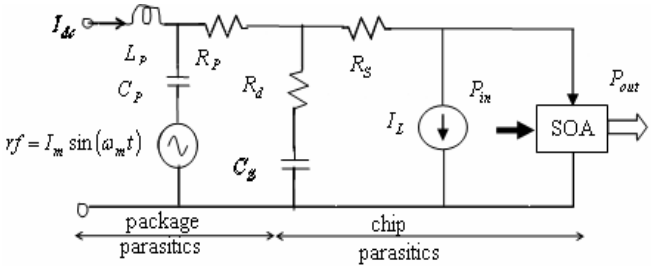

Fig.4: Circuit model incorporating different chip parasitic elements of SOA.

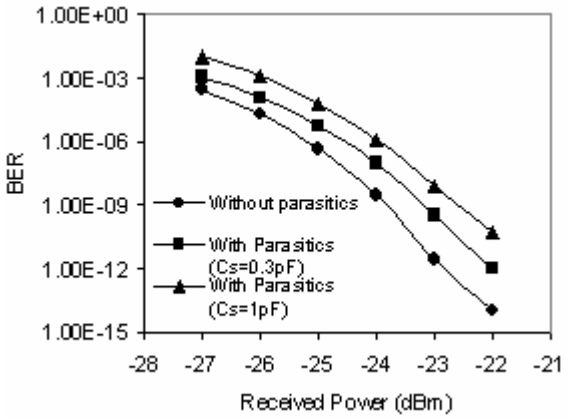

Fig.5: BER plot at 10Gbps with variation in received power in the presence of parasitic elements in the equivalent circuit model.

BER values at the output of the switch in CROSS and BAR state obtained from simulation of our model have been compared with the experimentally measured values[2]. Close agreement of both the results (as in Fig.3) indicates the validity of our model. Effect of inclusion of parasitic elements in the equivalent electrical circuit model of SOA as shown in Fig.4 (details of parasitics could be found in [3]) imposes a limit over the entire operating speed of the switch thereby resulting into a degradation in BER performance of the switch. As found from Fig.5 incorporation of shunt capacitance (C_S) of 1 pF and series resistance (R_S) of 100 ohm incurs almost 1.5 dB power penalty at BER of 10^{-9} at an operating speed of 10Gbps. The designer may find the model useful and handy for SOA based combinatorial logic design in a complex photonic network.

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